internal signal in accordance with a current flowing through the first and second transistors; and

a current regulating circuit connected to the differential circuit, wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.--

REMARKS

The Office Action dated February 13, 2001, has been received and carefully noted. The above amended claim and the following remarks are submitted as a full and complete response thereto.

Applicant thanks Examiner Le for granting Applicant a personal interview on May 8, 2001. The following remarks were discussed during the interview.

As a preliminary matter, Applicant respectfully submits that some of the information on Form PTO-892 which accompanied the First Office Action dated September 12, 2000, is incorrect. In particular, the patent number cited for Fernandez et al. was "5,448,209," and should be --5,448,200--. Additionally, the "Date" referred to for Harris et al. was indicated as "9/1998." Applicant respectfully submits that the correct date is --December 12, 1995 or 12/1995--. Applicant has attached a marked-up Form PTO-892 indicating the corrections made therein. Therefore, Applicant respectfully requests the issuance of a new Form PTO-892 with the corrections made therein.

Applicant appreciates allowed claims 6-20. Claim 1 has been amended. No new matter has been added by the above amended claim. Accordingly, claims 1-5 are respectfully submitted for consideration.

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Harris et al. (U.S. Patent No. 5,475,323, hereinafter "Harris"). In making this rejection, the Examiner took the position that Harris disclosed each and every element of the claimed invention with the exception of showing the input terminals being connected to a reference voltage and an external signal, respectively. The Examiner stated that it would have been obvious to a person of ordinary skill in the art "to apply an external signal and a fixed reference input voltage to the input terminals of Harris for purpose of operating the circuit as a threshold comparator." Furthermore, the Examiner took the position that the internal signal is generated at node 914 of Harris and that the current generator circuit 912 and 906 regulates the differential current of the amplifier responsive to the internal signals at node 914. Applicant respectfully submits that the above amended claim 1 overcomes the rejection, and submits that each of claims 1-5 recites subject matter which is neither disclosed nor suggested in the cited prior art.

Claim 1 recites an input circuit comprising a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates an internal signal in accordance with a current flowing through the first and second transistors. In addition, the input circuit comprises a current regulating circuit connected to the differential circuit, wherein the current regulating circuit

increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

Accordingly, the essence of the present invention is an input circuit having a current regulating circuit connected to the differential circuit wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit. As such, the present invention provides input circuits which amplify external signals to generate internal signals having predetermined amplitudes. Furthermore, the present invention results in the advantage of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claim 1, and therefore, fails to provide the critical and non-obvious advantages which are provided by the present invention.

Harris discloses an integrated circuit apparatus and method providing for utilizing voltage dividers and differential amplifiers. Harris discloses three integrated circuit resistors R_1, R_2 and R_3. The resistors have a length L_1, L_2 and L_3, and width W_1, W_2 and W_3, respectively. The voltage drop between node 101 and node 100 is Vin, the voltage drop between node 102 and node 100 is $Vout_1$, and the voltage drop between node 103 and node 100 is $Vout_2$. Harris also discloses a microelectronic resistor voltage divider 20 with linearly spaced output taps. In order to contact the voltage divider 20, accessible

outputs or tap connections are provided. Adding taps to voltage divider 20 will result in the creation of parasitic tap resistance between tap connection sites 28 and 30 and main body 34 of voltage divider 20. The effect of a tap is to place parasitic resistors, r_t associated with tap in parallel with small resistor segments, r_a, of the body of the resistor that is affected by r_t. Furthermore, Harris discloses that signal distortion problems due to a common mode signal are minimized through the use of common mode feedback control circuitry 912. Common mode feedback control circuitry 912 is also connected to current sources 900 and 902 and senses the currents and nodes 914. In response to the sensed currents, common mode feedback control circuitry adjusts a variable current source 906. Variable current source 906 sinks a varying current to V_{ssa} such that the current through transistors 1000 and 1010 is maintained at constant I_D even under common mode signal conditions and independent of variations in the current source.

Upon review and consideration of Harris, Applicant respectfully submits that each and every element recited within claim 1 of the present application is neither disclosed nor suggested by the cited prior art, and that the subject matter recited in claim 1 is not obvious to one of ordinary skill in the art in view of Harris. In particular, Applicant respectfully submits that the input circuit having current regulating transistors recited in the present application is clearly distinct and not obvious from that which is illustrated in Harris because Harris fails to disclose or suggest the limitation of a current regulating circuit connected to the differential circuit, wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating

circuit. The present invention provides that when the internal signal rises, the current regulating circuit (TN 4) increases an amount of the current flowing through the differential circuit and when the internal signal falls, the current regulating circuit (TN 4) decreases an amount of the current flowing through the differential circuit. Such configuration of the present invention improves a delay time of a signal output from the input circuit. In contrast, Harris merely discloses controlling of the variable current source 906 using the feedback control circuit 902, but does not teach or suggest the direct control of the variable current source using an internal signal. Furthermore, Harris' feedback control circuit 912 merely controls the variable current source 906 such that the current through transistors 1000, 1010 is maintained at a constant. (See column 17, lines 50-56 of Harris). In view of the above, it is respectfully submitted that Harris fails to disclose or suggest a current regulating circuit for increasing and decreasing an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit. As such, Applicant respectfully submits that Harris fails to disclose or suggest each and every element recited within claim 1 of the present application, and further submits that the subject matter recited in claim 1 is not obvious to one of ordinary skill in the art in view of Harris.

With regard to claims 2-5, Applicant submits that each of these claims recites subject matter which is neither disclosed nor suggested by Harris, or is not obvious to one of ordinary skill in the art in view of Harris. In particular, each of claims 2-5 depends on claim 1, and therefore, they inherently incorporate each and every element recited within claim 1 therein. Therefore, Applicant respectfully submits that each of claims 2-5 also

recites subject matter which is neither disclosed nor suggested by Harris, or is not obvious to one of ordinary skill in the art in view of Harris, for at least the reasons set forth above with respect to claim 1.

In view of the above, Applicant respectfully submits that claims 1-5, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1-5 be found allowable, and that this application with claims 1-20 be passed to issue.

If for any reason, the Examiner determines that this application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,
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MARKED-UP COPY OF ORIGINAL CLAIM 1

--1. (Twice Amended) An input circuit comprising:

a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates an internal signal in accordance with a current flowing through the first and second transistors; and

a current regulating circuit connected to the differential circuit, wherein the current regulating circuit [regulates] increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.--